

# Introduction to Computer Buses

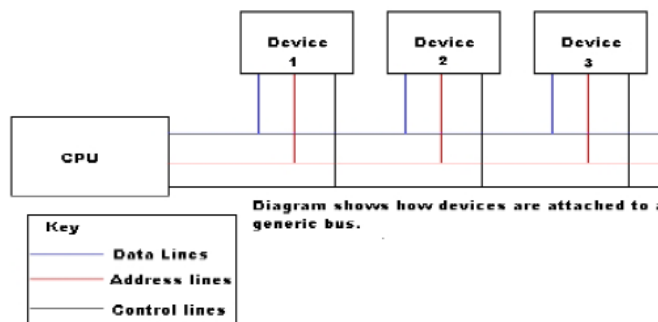
## References:

- The Intel Microprocessors, Bary B. Brey, 2007
- PCI System Architecture, Tom Shanley & Don Anderson



## Local Bus

- A set of parallel conductors, which allow devices attached to it to communicate with the CPU.
- The bus consists of three main parts:
  - Control lines, Address lines , Data lines



## Bus Protocols

- Requirements of a BUS standard
  - Electrical, Mechanical requirements
  - Protocol requirements
- Common BUS standards
  - ISA and EISA
  - MCA (Micro Channel Bus)
  - VESA Local BUS (Video Electronic Standard Associations) – 1-2 devices can be connected.
  - PCI Local BUS



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## ISA (Industry Standard Architecture)

- Has a clock speed limit of 8 MHz
- Has a word length of 8 or 16 bits (8 or 16 data lines)
- Requires two clock ticks to transfer data (16 bit transfers)
- Very slow for high performance disk accesses and high performance video cards

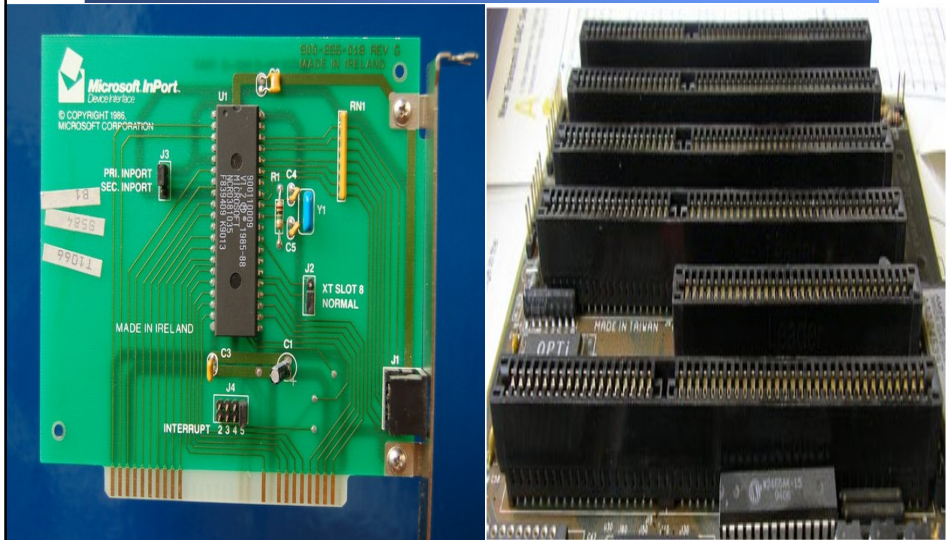


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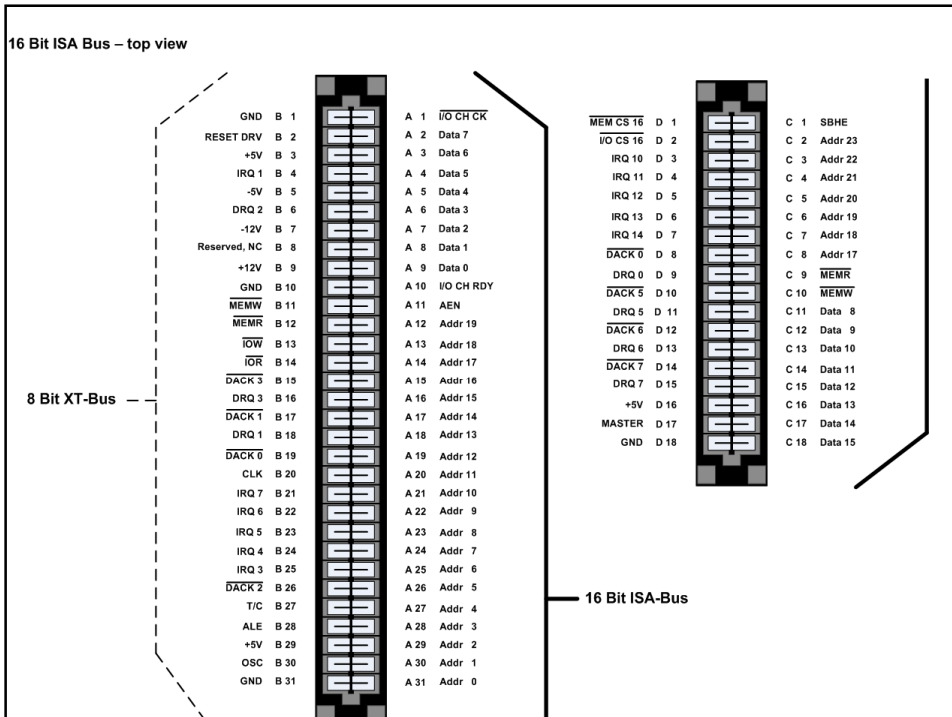
# ISA (Industry Standard Architecture)



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## EISA (Enhanced ISA)

- Has a clock speed of 8.33 MHz
- Maximum of a 32-bit wide word length(32 data lines)
- Can support lots of devices
- Supports older devices which have Slower or Smaller word lengths(ISA)
- Transfers data every clock tick.



## MCA (Micro-Channel Bus)

- Has a clock speed of 10 MHz
- Has a 32 bit word length (32 data lines)
- Transfers data every clock tick.



## VESA (Video Electronic Std Arch.)

- Has a clock speed limit of 33 MHz.
- Limited to a 32-Bit wide word length (32 data lines).
- Cannot take advantage of the Pentium's 64 bit architecture.
- Limited support for Burst Transfers, thereby limiting the achievable thruput.
- Restricted on the number of devices which can be connected ( 1 or 2 devices).

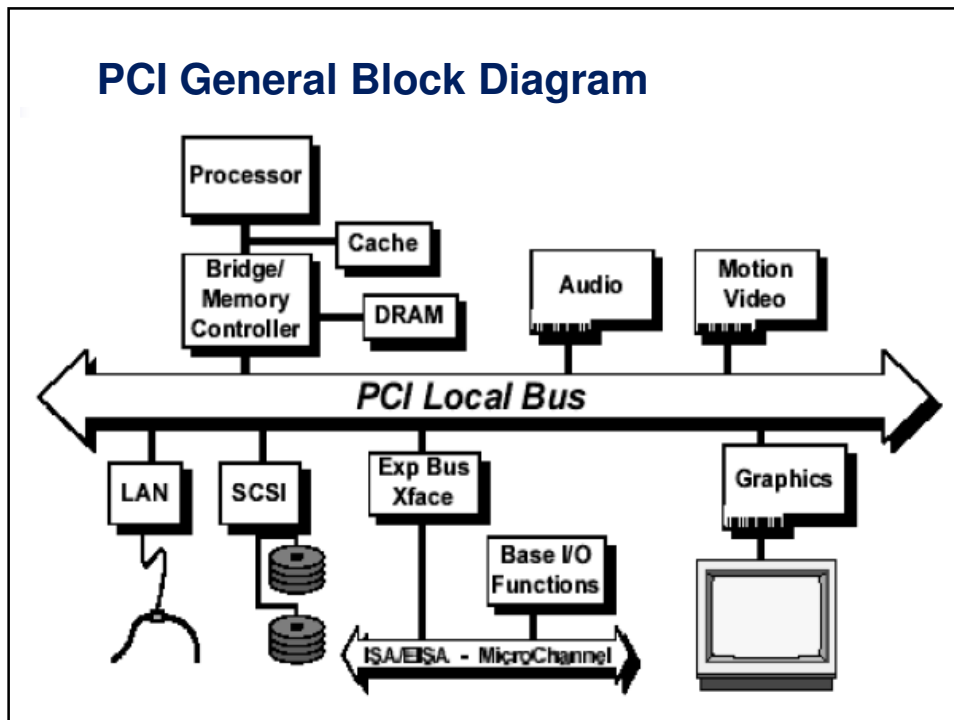


## PCI Local Bus

- Bus Width – 32 or 64 bits
- Operating frequency > 100 MHz
- Can support many more devices than VESA
- 64 bit extension for Pentium proc.
- Greater Variety of Expansion cards available.
- Multiplexed Address and Data
- PCI SIG (Special Interest Group)



## PCI General Block Diagram



## SCSI Peripheral Device

A SCSI Peripheral Device Type is a five-bit field which was defined in the very early days of SCSI. The possible values are:

- 00h - direct-access device (e.g., magnetic disk)
- 01h - sequential-access device (e.g., magnetic tape)
- 02h - printer device
- 03h - processor device
- 04h - write-once device
- 05h - CDROM device
- 06h - scanner device
- 07h - optical memory device (e.g., some optical disks)
- 08h - medium Changer (e.g. jukeboxes)
- 09h - communications device
- 0Ah-0Bh - defined by ASC IT8 (Graphic arts pre-press devices)
- 0Ch - Storage array controller device (e.g., RAID)
- 0Dh - Enclosure services device
- 0Eh - Simplified direct-access device (e.g., magnetic disk)
- 0Fh - Optical card reader/writer device
- 10h - Reserved for bridging expanders
- 11h - Object-based Storage Device
- 12h - Automation/Drive Interface
- 13h-1Dh - reserved
- 1Eh - Well known logical unit
- 1Fh - unknown or no device type

## PCI Local Bus Features

- **Performance –**
  - Burst Transfer at 528 MBps peak (64 bit- 66 MHz)
  - Fully concurrent with Processor-Memory subsystem
  - Access time is as fast as 60ns.
  - Hidden central arbitration.
- **Low cost – multiplexed, no glue logic**
- **Low Pin count – 47 pin for target; 49 pin as initiator.**
- **Ease of Use – full auto configuration**
- **Flexibility – processor independent, accommodates other protocols**
- **Green Machine ‘CMOS drivers -> low power**



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## PCI Devices and PCI Cores

- **Every device on the PCI bus is either**
  - PCI compliant – has the same signals as the PCI bus
  - Connected via a PCI core – this piece of hardware does the interfacing
- **Common devices**
  - Audio/Video cards
  - LAN cards
  - SCSI controllers

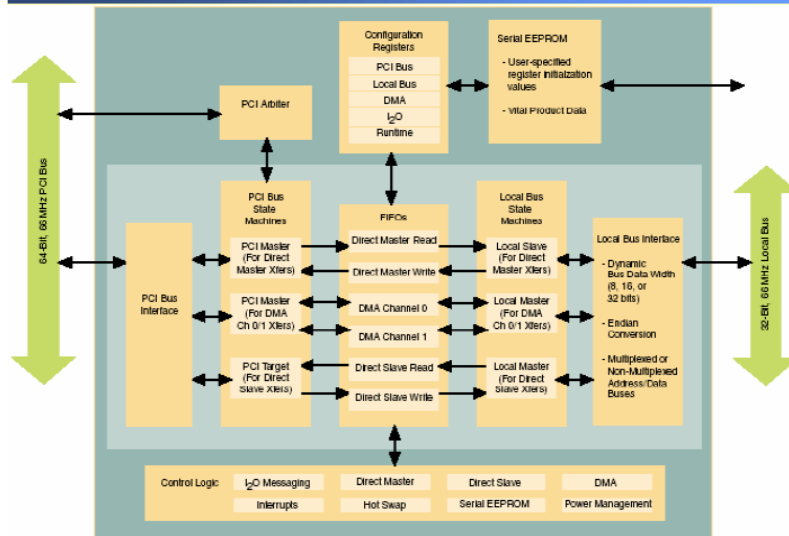


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## PCI Core – 9656BA



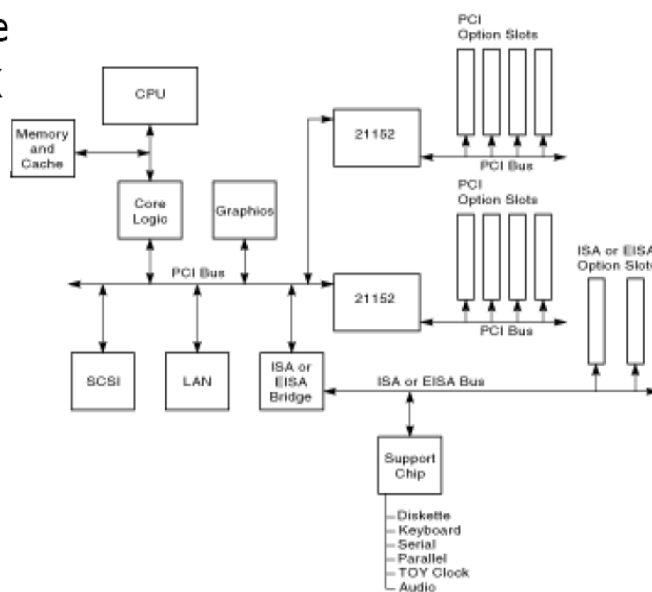
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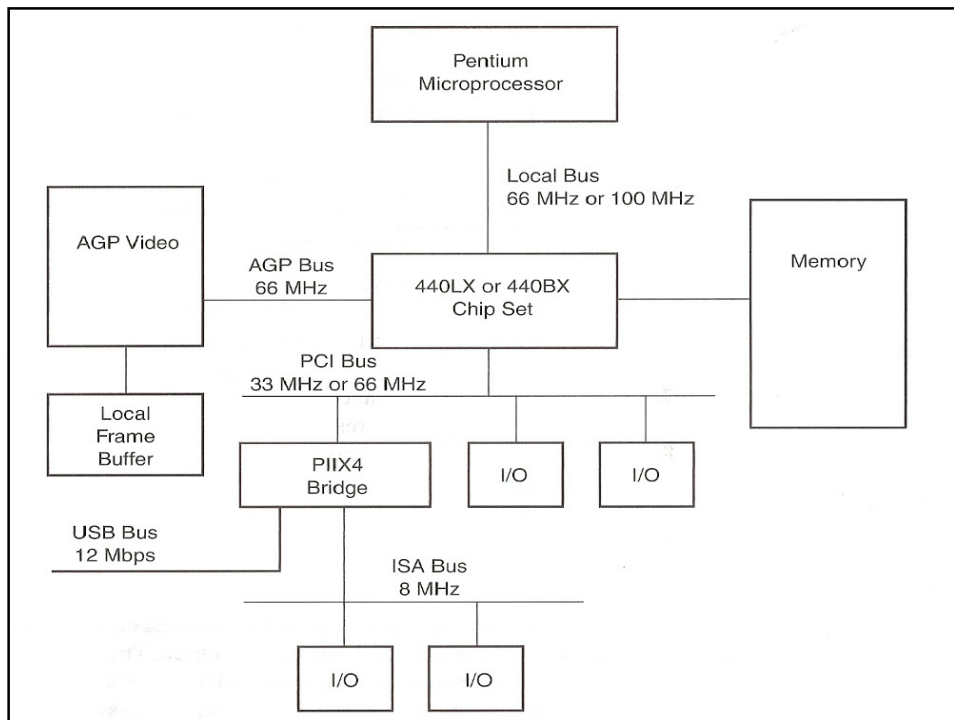
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## Multiple Bus

- PCI to PCI bridge
- Concept of LOCK
- All on one level



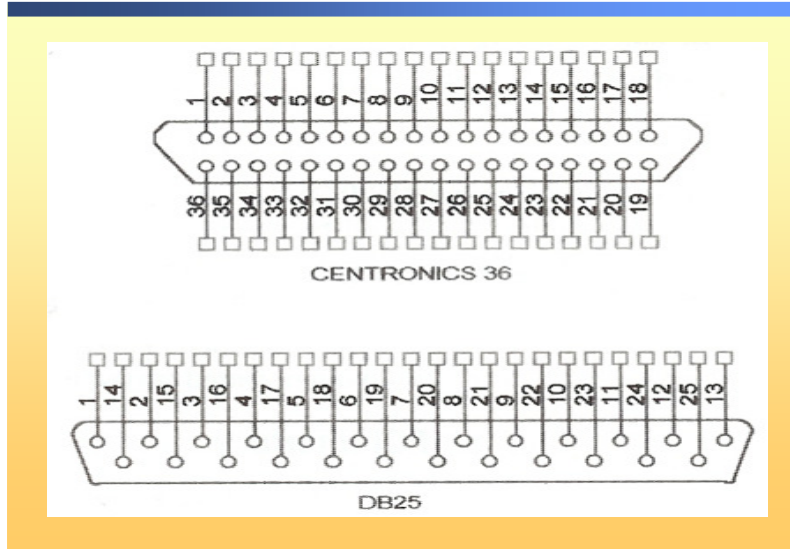


## The Parallel Port

- **The parallel port is a legacy device that was at one time used to send data to printers.**
- **Most printers today are USB devices because of the reduced cost of the cable.**
- **Parallel can sustain data rates that approach 500 MBps.**



# The Parallel Port



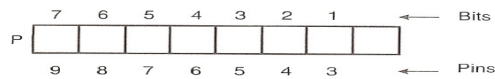
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# The Parallel Port

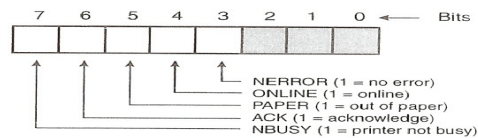
## Port 378H

The data port that connects to bits D0–D7 (pins 2–9)

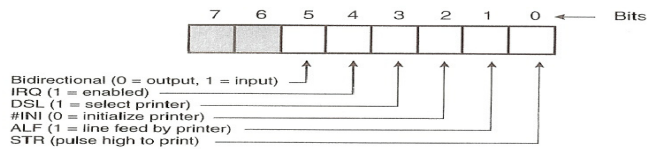


## Port 379H

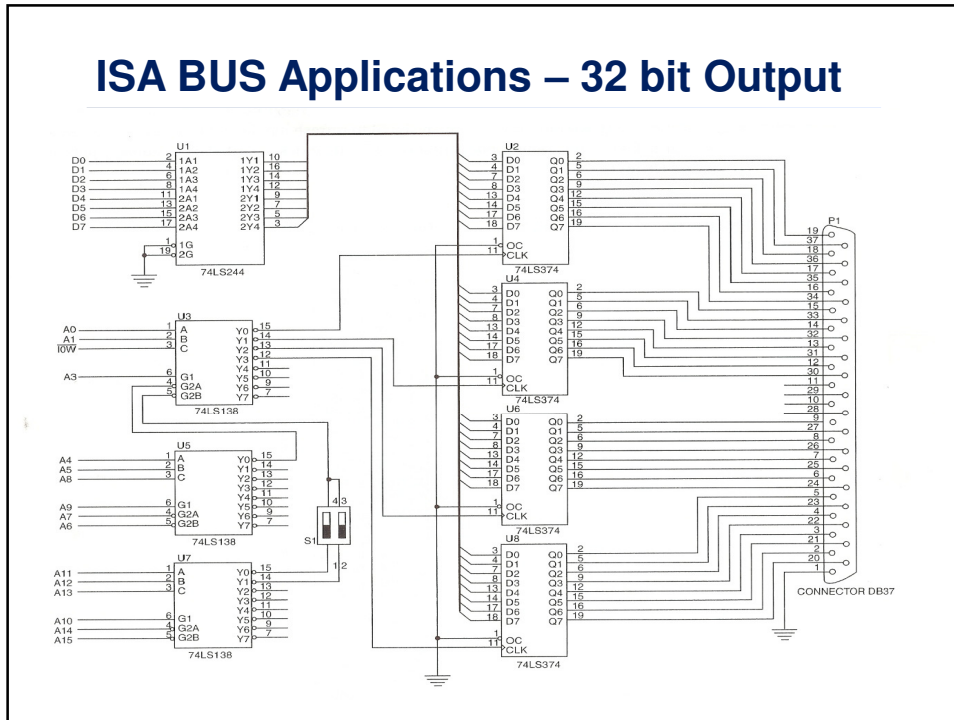
This is a read-only port that returns the information from the printer through signals such as BUSY, #ERROR, and so forth. (Careful! Some of the bits are inverted.)



## Port 37AH



## ISA BUS Applications – 32 bit Output

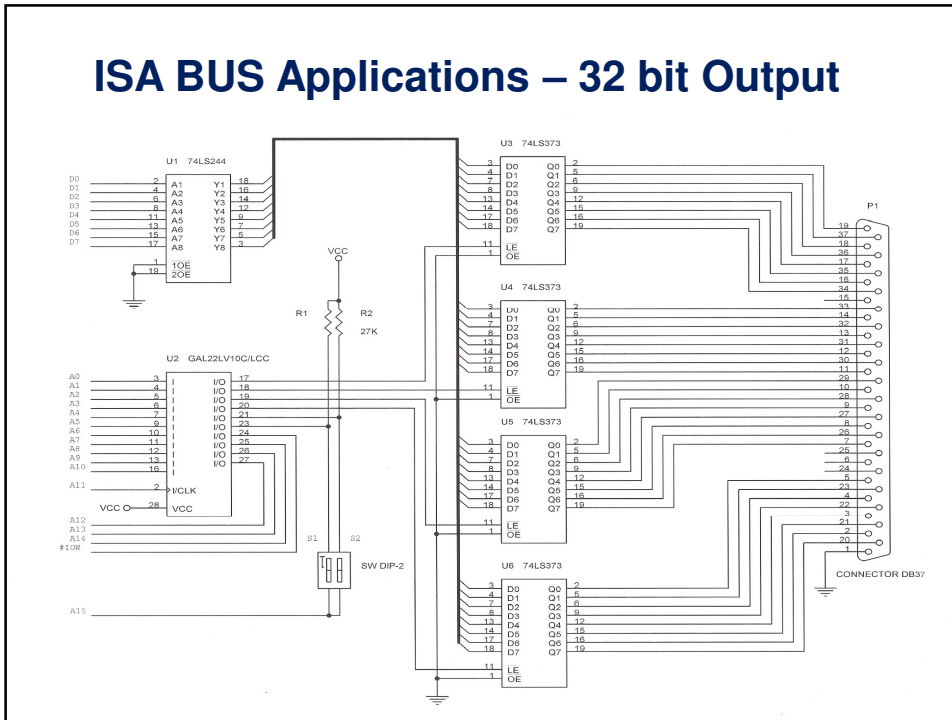


## ISA BUS Applications – 32 bit Output

DIP Switch	Latch U2	Latch U4	Latch U6	Latch U8
1-4 On	0608H or 060CH	0609H or 060DH	060AH or 060EH	060BH or 060FH
2-3 On	0E08H or 0E0CH	0E09H or 0E0DH	0E0AH or 0E0EH	0E0BH or 0E0FH



## ISA BUS Applications – 32 bit Output



## ISA BUS Applications – 32 bit Output

S2	S1	U3	U4	U5	U6
On	On	0300H	0301H	0302H	0303H
On	Off	0304H	0305H	0306H	0307H
Off	On	0308H	0309H	030AH	030BH
Off	Off	030CH	030DH	030EH	030FH



```

library ieee;
use ieee.std_logic_1164.all;
entity DECODER_15_3 is
port (
    IOW, A14, A13, A12, A11, A10, A9, A8, A7, A6
        A5, A4, A3, A2, A1, A0, S1, S2: in STD_LOGIC;
    U3, U4, U5, U6: out STD_LOGIC
);
end;
architecture V1 of DECODER_15_3 is
begin
    U3 <= IOW or A14 or A13 or A12 or A11 or A10 or not A9 or not A8 or A7
        or A6 or A5 or A4 or A1 or A0 or (S2 or S1 or A3 or A2) and (S2 or
        not S1 or A3 or not A2) and (not S2 or S1 or not A3 or A2) and
        (not S2 or not S1 or not A3 or not A2);
    U4 <= IOW or A14 or A13 or A12 or A11 or A10 or not A9 or not A8 or A7
        or A6 or A5 or A4 or A1 or not A0 or (S2 or S1 or A3 or A2) and
        (S2 or not S1 or A3 or not A2) and (not S2 or S1 or not A3 or A2)
        and (not S2 or not S1 or not A3 or not A2);
    U5 <= IOW or A14 or A13 or A12 or A11 or A10 or not A9 or not A8 or A7
        or A6 or A5 or A4 or not A1 or A0 or (S2 or S1 or A3 or A2) and
        (S2 or not S1 or A3 or not A2) and (not S2 or S1 or not A3 or A2)
        and (not S2 or not S1 or not A3 or not A2);
    U6 <= IOW or A14 or A13 or A12 or A11 or A10 or not A9 or not A8 or A7
        or A6 or A5 or A4 or not A1 or not A0 or (S2 or S1 or A3 or A2)
        and (S2 or not S1 or A3 or not A2) and (not S2 or S1 or not A3 or
        A2) and (not S2 or not S1 or not A3 or not A2);
end V1;

```

