

Memory Interface

In this chapter, we explain how to interface both ROM and RAM to the Intel family of microprocessors.

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Objectives

- Upon completion of this chapter, you will be able to
 - Decode the memory address and use the outputs of the decoder to select various memory components.
 - Use programmable logic devices to decode memory addresses.
 - Explain how to interface both ROM and RAM to a microprocessor.
 - Interface memory to an 8-, 16-, 32- and 64-bit data bus.
 - Explain the operation of a dynamic RAM controller.
 - Interface dynamic RAM to the microprocessor.

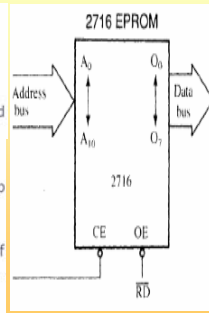
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Memory Devices

Memory Pin Connections:

- Address connections:
 - Address inputs that select a memory location within the memory device.
- Data connections:
 - Data outputs or input/outputs at which data are entered for storage or extracted for reading.
- Selection connections:
 - Signal inputs that selects or enables the memory device. (e.g. chip enable \overline{CE} , chip select \overline{CS} , select S etc.)
- Control connections:
 - Signal inputs that controls the operation of the memory device (e.g. write enable \overline{WE} , read enable \overline{RE} , output enable \overline{OE} , read/write R/\overline{W} etc.)



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Memory Devices

ROM Memory:

- The **read-only memory (ROM)** is permanently programmed so data are always present, even when power is disconnected.
- It is used to store programs and data that are resident to the system and must not change when power is disconnected.
- It is also called **nonvolatile memory**.
- The **EPROM (erasable programmable ROM)** is erasable if exposed to high-intensity ultraviolet light for about minutes.
- The **PROM (programmable ROM)** is programmed in the field by burning open tiny fuses, but once programmed it can't be erased.

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Memory Devices

ROM Memory:

- The **EEPROM (electrically erasable programmable ROM)** is electrically erasable in the system, but require more time to erase than a normal RAM.
- EEPROM is also called **flash memory**.
- This type of memory component requires wait states to operate properly with the 8088/8086 processors because of its rather long access time.

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Memory Devices

Static RAM:

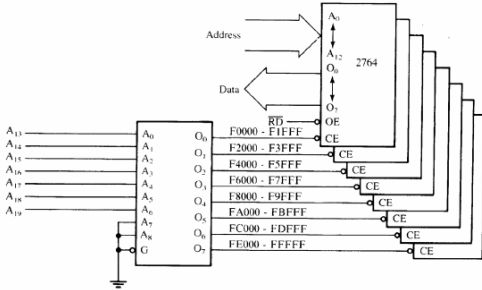
- It **retains data for as long as DC power is applied**.
- No special action (except power) is required to retain stored data.
- The access time of a SRAM is much shorter than that of a ROM, and no wait state is required in general.
- Examples include 4016(2K×8) and 62256(32K×8).

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Address Decoding

- Use PROM decoder:



A memory system using the TPB26L42, 512 x 8 PROM as an address

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Address Decoding

The 825147 PROM programming pattern for the illustrated circuit.

Inputs								Outputs									
OE	A8	A7	A6	A5	A4	A3	A2	A1	A0	O0	O1	O2	O3	O4	O5	O6	O7
0	0	0	1	1	1	1	0	0	0	1	0	1	1	1	1	1	1
0	0	0	1	1	1	1	0	0	1	1	0	1	1	1	1	1	1
0	0	0	1	1	1	1	0	1	0	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	0	1	1	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	1	0	0	1	1	1	1	0	1	1	1
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
all other combinations										1	1	1	1	1	1	1	1

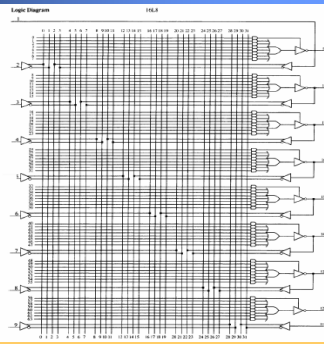
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Address Decoding

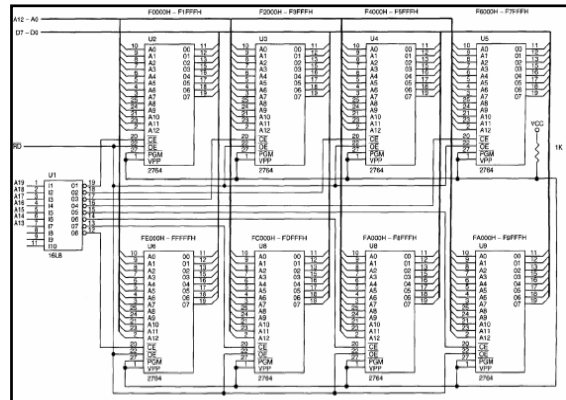
- Use PLD programmable decoders:

The PAL 16L8
(Advanced Micro Devices, Inc., 1988.)



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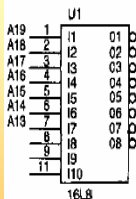


A PAL16L8 that decodes 8 2764 (8K x 8) memory devices

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Address Decoding Example



```

TITLE      Address Decoder
CHIP      DECODER1 PAL16L8

:pins 1 2 3 4 5 6 7 8 9 10
      A19 A18 A17 A16 A15 A14 A13 NC NC GND

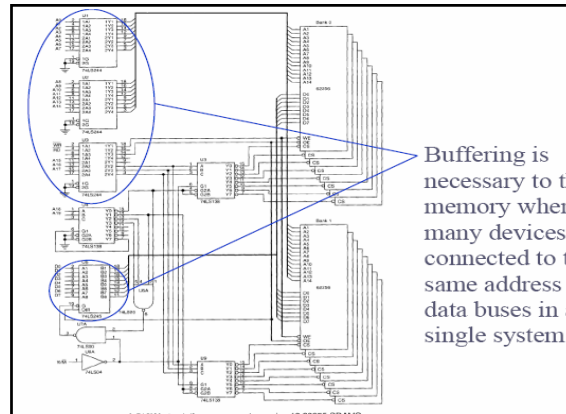
:pins 11 12 13 14 15 16 17 18 19 20
      NC O8 O7 O6 O5 O4 O3 O2 O1 VCC

EQUATIONS

/O1 = A19 * A18 * A17 * A16 * /A15 * /A14 * /A13
/O2 = A19 * A18 * A17 * A16 * /A15 * /A14 * A13
/O3 = A19 * A18 * A17 * A16 * /A15 * A14 * /A13
/O4 = A19 * A18 * A17 * A16 * /A15 * /A14 * A13
/O5 = A19 * A18 * A17 * A16 * A15 * /A14 * /A13
/O6 = A19 * A18 * A17 * A16 * A15 * A14 * /A13
/O7 = A19 * A18 * A17 * A16 * A15 * /A14 * A13
/O8 = A19 * A18 * A17 * A16 * A15 * /A14 * A13
    
```

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Buffering is necessary to the memory when many devices are connected to the same address and data buses in a single system.

A 512K byte static memory system using 16 82255 SRAMs

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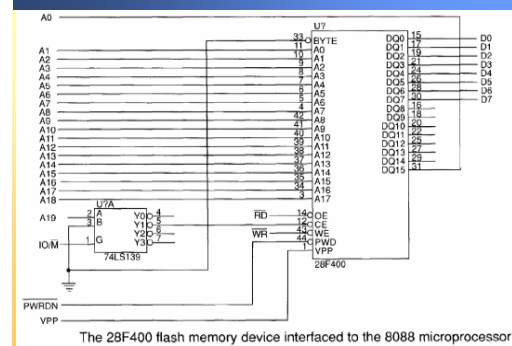
Interfacing Flash Memory to CPU

- Differences between a flash memory device and SRAM
 - the flash memory device requires a 12 V programming voltage (V_{pp}) to erase and write new data
 - the amount of time required to accomplish a write operation ($\sim 0.4s$ in flash memory c.w. $\sim 10ns$ in SRAM)

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Interfacing Flash Memory to CPU



The 28F400 flash memory device interfaced to the 8088 microprocessor

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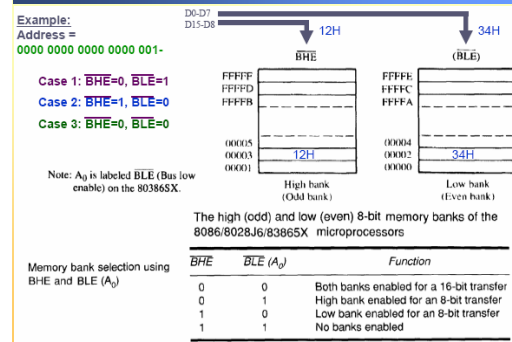
Interfacing Flash Memory to CPU

- The Intel 28F400 flash memory device can be used as either a 512Kx8 (byte mode) memory device or as a 256Kx16 (word mode) memory device, which is selected by the control pin BYTE.
- The pin DQ15 of 28F400 functions as the least significant address input when the device operates in the byte mode.

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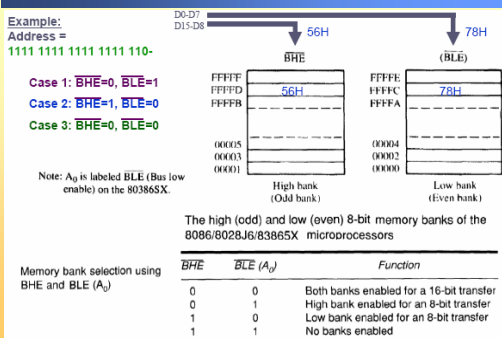
16-bit Memory Interface (8086/80286/80386SX)



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16-bit Memory Interface (8086/80286/80386SX)



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16-bit Memory Interface (8086/80286/80386SX)

- Bank selection can be accomplished in two ways:
 - Issue a separate write signal to select a write to each bank of memory.
 - Use separate decoders for each bank.
- No separate read signal is required for each memory bank as processors can select the data they need at any time from half of the data bus.

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16-bit Memory Interface (8086/80286/80386SX)

Separate Bank Decoders:

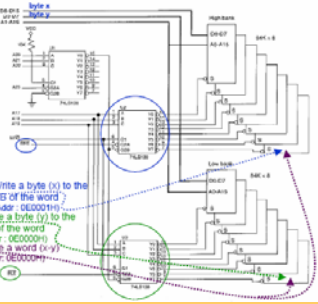
- It's more expensive and less effective.

Example:
Address =
0000 1110 0000 0000 0000 0000

Case 1: BHE=0, BLE=1

Case 2: BHE=1, BLE=0

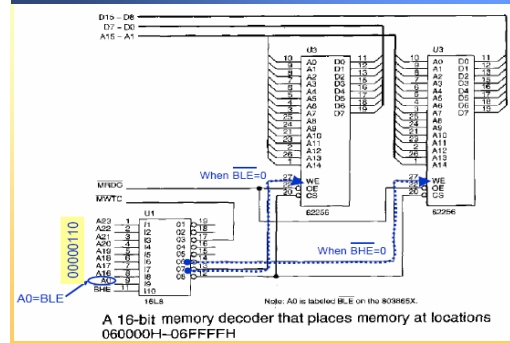
Case 3: BHE=0, BLE=0



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Example of a 16-bit Memory Interface



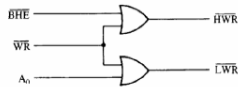
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16-bit Memory Interface (8086/80286/80386SX)

Separate Bank Write Strobes:

- It's more effective and less expensive.



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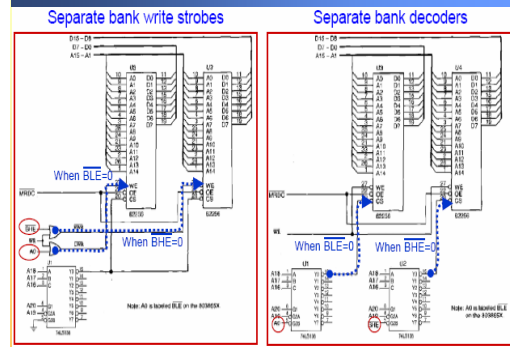
TITLE      Address Decoder
CHIP      DECODER2 PAL16L8
;pins 1 2 3 4 5 6 7 8 9 10
A23 A22 A21 A20 A19 A18 A17 A16 A0 GND
;pins 11 12 13 14 15 16 17 18 19 20
BHE SEL LWR HWR NC NC MWTC NC NC VCC

EQUATIONS
/SEL = /A23 * /A22 * /A21 * /A20 * /A19 * A18 * A17 * /A16
/LWR = /MWTC * /A0
/HWR = /MWTC * /BHE
    
```

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Example of a 16-bit Memory Interface

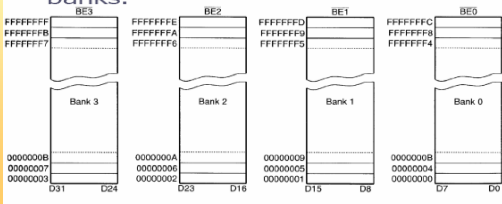


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32-bit Memory Interface (80386DX and 80486)

- Bank selection can be accomplished by the bank selection signals $\overline{BE3}$, $\overline{BE2}$, $\overline{BE1}$ and $\overline{BE0}$.
- A 8-, 16- or 32-bit number can be transferred by selecting appropriate banks.



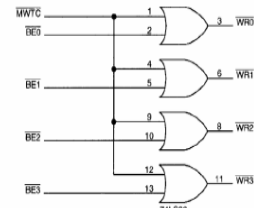
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32-bit Memory Interface (80386DX and 80486)

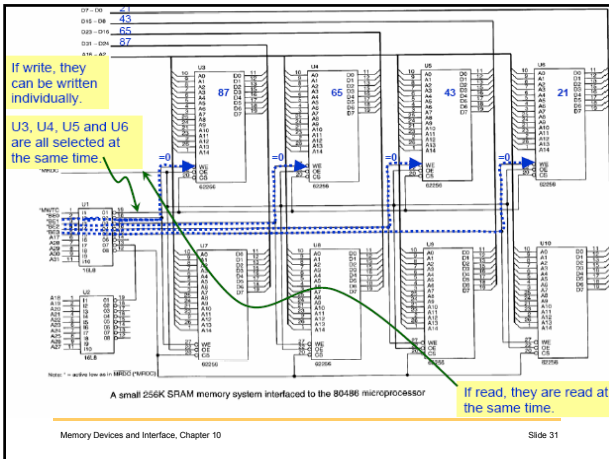
- Separate write strobe signals can be developed to select a write to each memory bank.

Bank write signals for the 80386DX and 80486 microprocessors



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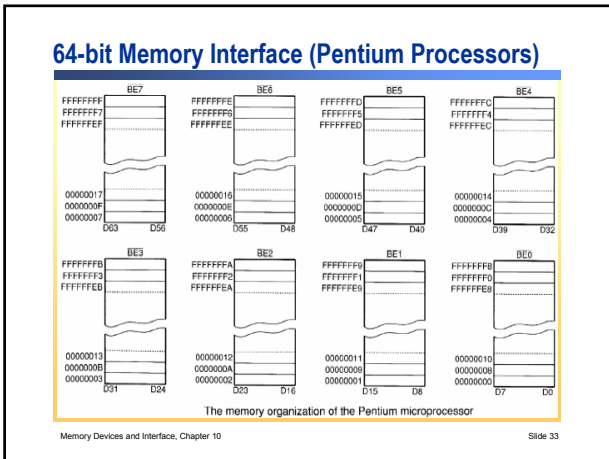
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64-bit Memory Interface (Pentium Processors)

- Bank selection is accomplished by the bank selection signals $\overline{BE7}$, $\overline{BE6}$, $\overline{BE5}$, $\overline{BE4}$, $\overline{BE3}$, $\overline{BE2}$, $\overline{BE1}$ and $\overline{BE0}$.
- A 8-, 16-, 32- or 64-bit number can be transferred by selecting appropriate banks.

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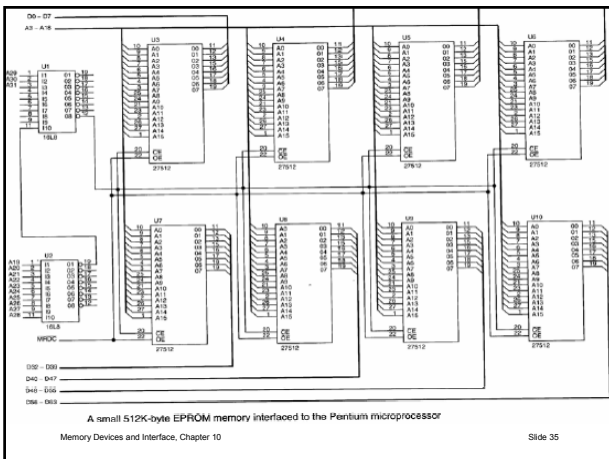


64-bit Memory Interface (Pentium Processors)

The separate write strobe signals can be obtained by combining the bank selection signals with the /MWTC signal, which is generated by combining the M/I/O and W/R.

The generation of the write strobes for the Pentium microprocessor

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Dynamic RAM

- As RAM memory is often very large, sometimes it is desirable to use DRAMs instead of SRAMs to **reduce the system cost**.
- A DRAM **retains data for only 2-4 ms** and **requires the multiplexing of address inputs**.
- DRAM **must be refreshed periodically**.

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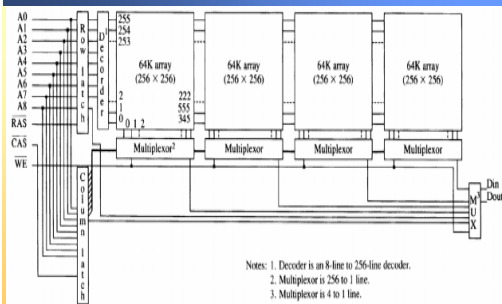
Dynamic RAM

- A refresh can be accomplished by doing a read, a write, or a special refresh cycle that doesn't read or write data.
- A refresh cycle which is totally internal to the DRAM is called either **hidden refresh**, **transparent refresh**, or sometimes **cycle stealing**.
- In a **hidden refresh**, an RAS-only cycle strobes a row address into the DRAM to select a row of bits to be refreshed, and, at the same time, the RAS input also causes the selected row to be read out internally and rewritten into the selected bits.

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Internal Structure of a Dynamic RAM



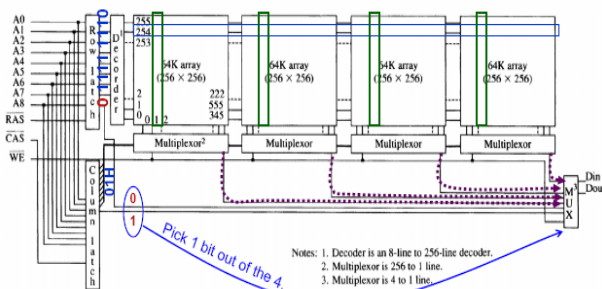
The internal structure of a 256K x 1 DRAM. Note that each of the internal 256 words are 1,025-bits wide.

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- Step 1: Give a 9-bit row addr (e.g. 0 1111 1110B)
Step 2: Give a 9-bit col addr (e.g. 1 0000 0001B)
Step 3: Get a bit

Read Example



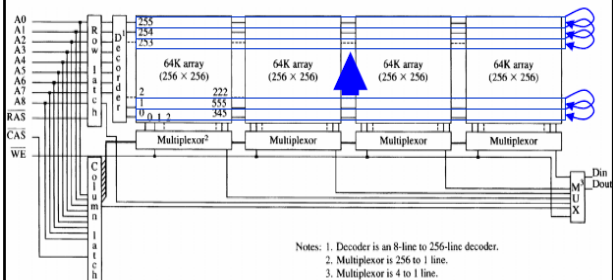
The internal structure of a 256K x 1 DRAM. Note that each of the internal 256 words are 1,025-bits wide.

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Refresh Example

- Step 0: DRAM controller initializes ROW addr counter = 0
Step 1: Give a 9-bit row addr by a DRAM controller
Step 2: read & write the row internally
Step 3: the DRAM controller increases the ROW addr by 1
Step 4: IF ROW addr < 256 GOTO step 1, else GOTO step 0



The internal structure of a 256K x 1 DRAM. Note that each of the internal 256 words are 1,025-bits wide.

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Refresh Overhead

- The row address is usually obtained from a binary counter.
- An **overhead is required** to perform the refresh when exploiting the DRAM.
- In a 8088/8086 system running at a **5 MHz** clock, it takes **800 ns** to do a refresh.
- If there are **256 rows** to be refreshed within **4 ms**, then the refresh cycle must be activated at least once every $4\text{ms}/256 = 15.6\mu\text{s}$ to meet the specification.
- In other words, it takes 800ns to refresh every 15.6ms.
- Hence, the **overhead** = $0.8/15.6 \approx 5.13\%$.

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Refresh Overhead

- In a modern microprocessors such as a **3.0 GHz Pentium IV**, the period of **15.6μs** is a great deal of time!
- Since this **Pentium IV** executes an instruction in about **one-third ns**, the refreshment overhead is much less than 1%, as shown below:

$$\text{Overhead Time}\% = \frac{0.333 \text{ ns}}{15.6 \mu\text{s}} \times 100\% = \frac{111}{52000}\%$$

$$\text{Overhead Time}\% \approx 0.0021\%$$

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EDO Memory

- EDO (Extended data Output) RAM is a modified version of DRAM. In this type of memory, any memory access, including a refresh, stores the selected row of bits into latches. Thus, in most programs, which are sequentially executed, the row of latched data are available without any wait states.
- This slight modification to the internal architecture of the DRAM increases system performance by about 15 to 25%.
- Although EDO memory is no longer available, this technique is still employed in all modern DRAM chips (SDRAM and DDRAM).

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The Intel 82C08 DRAM Controller

- The Intel 82C08 DRAM controller can control up to 2 banks of 256Kx16 DRAM memory (i.e. 1M byte of memory).
- The 82C08 contains an address multiplexer that multiplexes an 18-bit address onto 9 address connections for 256K memory devices and circuitry that generates $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals for the DRAM.

5	AL0	AD0	7
6	AL1	AD1	8
7	AL2	AD2	9
8	AL3	AD3	10
9	AL4	AD4	11
10	AL5	AD5	12
11	AL6	AD6	13
12	AL7	AD7	14
13	AL8	AD8	15
14	AL9	AD9	16
15	AL10	AD10	17
16	AL11	AD11	18
17	AL12	AD12	19
18	AL13	AD13	20
19	AL14	AD14	21
20	AL15	AD15	22
21	AL16	AD16	23
22	AL17	AD17	24
23	AL18	AD18	25
24	AL19	AD19	26
25	AL20	AD20	27
26	AL21	AD21	28
27	AL22	AD22	29
28	AL23	AD23	30
29	AL24	AD24	31
30	AL25	AD25	32
31	AL26	AD26	33
32	AL27	AD27	34
33	AL28	AD28	35
34	AL29	AD29	36
35	AL30	AD30	37
36	AL31	AD31	38
37	AL32	AD32	39
38	AL33	AD33	40
39	AL34	AD34	41
40	AL35	AD35	42
41	AL36	AD36	43
42	AL37	AD37	44
43	AL38	AD38	45
44	AL39	AD39	46
45	AL40	AD40	47
46	AL41	AD41	48
47	AL42	AD42	49
48	AL43	AD43	50
49	AL44	AD44	51
50	AL45	AD45	52
51	AL46	AD46	53
52	AL47	AD47	54
53	AL48	AD48	55
54	AL49	AD49	56
55	AL50	AD50	57
56	AL51	AD51	58
57	AL52	AD52	59
58	AL53	AD53	60
59	AL54	AD54	61
60	AL55	AD55	62
61	AL56	AD56	63
62	AL57	AD57	64
63	AL58	AD58	65
64	AL59	AD59	66
65	AL60	AD60	67
66	AL61	AD61	68
67	AL62	AD62	69
68	AL63	AD63	70
69	AL64	AD64	71
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74	AL69	AD69	76
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97	AL92	AD92	99
98	AL93	AD93	100
99	AL94	AD94	101
100	AL95	AD95	102
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102	AL97	AD97	104
103	AL98	AD98	105
104	AL99	AD99	106
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107	AL102	AD102	109
108	AL103	AD103	110
109	AL104	AD104	111
110	AL105	AD105	112
111	AL106	AD106	113
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155	AL150	AD150	157
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